REMARKS

These remarks are in response to the final Official Action mailed on February 12, 2002. Consequently, the present Amendment is being filed with a Request for Continued Examination (RCE). The Office Action rejected claims 37 and 39-45 under 35 U.S.C. 112, first paragraph. In particular, the Office Action states maintains its rejection of the previous Office Action, namely that it fails to find support in the present application for the process of "programming the memory cell until the charge of the memory cell is above the programmed-cell reference level." This is respectfully submitted to be in error. Further, claims 42-45, that were added in the previous Amendment do not contain this limitation so that there appears to be no grounds for the rejection of these claims. Similarly, claims 39 and 40 contain differing language from claim 37. These claims and the reasons why the rejections are believed to be in error are discussed below. Additionally, the filing of an RCE with this Amendment is being taken advantage of to add several new claims, as is also discussed below.

Claims 42-45

The Office Action rejected claims 42-45 for the same grounds as in the previous Office Action. Claims 42-45 were added in the previous Amendment and were not pending at the time of the previous Office Action. Furthermore, the specific reason stated for the rejection of claim 42-45 (as well as the other pending claims) is a lack of support for the restriction "programming the memory cell until the charge of the memory cell is above the programmed-cell reference level", a restriction which is not contained in claims 42-45. Consequently, there are no grounds for the rejection of these claims in the Office Action and claims 42-45 should be allowed.

As for support of what is contained in claims 42-45, claim 42 states:

> A method of improving data retention in a nonvolatile writable memory having a first reference level and a second reference level, the nonvolatile writable memory having a plurality of memory cells, each of the memory cells being in an first state when storing a charge below the first reference level, and each of the memory cells being in a second state when storing a charge above the second reference level, the method comprising:
>
> writing into each of a set of the plurality of memory cells a respective data value, wherein the data values are one of the first and second states;
>
> identifying a memory cell of the set having a charge above the first reference level and below the second reference level; and
>
> rewriting the respective data value into the memory cell.

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This claim is believed to be fully supported by the specification of the present application. In particular, this is process of Figures 8-10 and their corresponding description.

The "writing into each of a set of the plurality of memory cells a respective data value, wherein the data values are one of the first and second states" is shown in Figure 8, with step 801 "WRITE DATA", with steps 802-807 dedicated to verifying that the cells have been correctly written. Step 808 is the scrub process, shown in more detail in Figure 9: Steps 901 (setting voltage and reading) and 902 ("READ OK?") determine if a cell's charge level of the set is "below the second reference level" and steps 903 (setting voltage and reading) and 904 ("READ OK?") determine if a cell of the set is "above the first reference level". (The relation of the various voltages is shown in Figure 10.) If the answer is NO in either step 902 or 904, the cell is "above the first reference level and below the second reference level" and the "rewriting the respective data value into the memory cell" occurs is step 905 ("REWRITE DATA BACK TO MEMORY").

Thus, it is believed that independent claim 42 is fully supported and that a rejection of this claim and dependent claims 43-45 under 35 U.S.C. 112, first paragraph, is with foundation. Dependent claims 43 and 44 concern using a "scrub high" and a "scrub low" voltage that lie within the verify voltages, as is shown in Figure 10. Claim 45 concerns the use of error correction code (ECC) in the rewrite process. All of these dependent claims are also fully supported in the present application.

New Claims

Newly added claims 46-50 are also drawn to the "scrub operation" aspect of the present application as described beginning on page 24, line 29. The use of a scrub during a read operation is described beginning on page 25, line 27.

Claims 37 and 39-41

The Office Action has maintained its rejection under 35 U.S.C. 112, first paragraph. In particular, the Office Action again fails to find support in the present application for the process of "programming the memory cell until the charge of the memory cell is above the programmed-cell reference level." The Applicants believe that support for this process is clearly presented in the present application and are unclear as to what in particular is found lacking. In particular, the Office Action states that it fails to find "proper antecedent support" and it is unclear to what the "antecedent" is in reference.

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In the scrubbing process of Figure 9, step 905 is clearly a programming step that would be "programming the memory cell". The programming process shown in Figure 8 has, in steps 801, 802, 803 and 809, a program/verify loop. This results in the cell having a threshold value above the programmed-cell reference level, namely V_{PV} (or alternately V_{PRH} or V_{SH} depending on the embodiment, where these values are illustrated in Figure 10). The read value of a floating gate memory cell at a reference voltage during the verify process is indicative of the charge of the memory cell, as is described, for example, beginning on page 2, line 17, of the application and is standard in the operation of such cells. Consequently, the programming of the memory cell in the loop of steps 801, 802, 803, and 809 is "until the charge of the memory cell is above the programmed-cell reference level." Thus, the process of "programming the memory cell until the charge of the memory cell is above the programmed-cell reference level" is fully supported in the present application.

Consequently, the rejection of claim 37 and its dependent claim 41 is respectfully submitted to be without foundation. Claims 39 and 40 are drawn to the same aspect of the present invention and are similarly believed allowable.

Conclusion

Therefore, it is respectfully submitted that the present application fully supports the claimed subject matter and that a rejection under 35 U.S.C. 112, first paragraph, is not well founded, and that claims 37 and 39-45 are allowable. Reconsideration of the Office Action's rejection of claims 37 and 39-45, consideration of new claims 46-50, and a prompt declaration of the previously requested interference is respectfully requested. The undersigned will attempt to follow up this Amendment with a telephone call in order to discuss these rejections in case further clarification is needed. In the meantime, however, if the Examiner has any questions about this request, application, or response, a telephone call to the undersigned is invited.

EXPRESS MAIL LABEL NO:

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Respectfully submitted,

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5/9/02

Date

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APPENDIX

Pending Claims

(Claims 35 and 36 have been cancelled)

37. A method of improving data retention in a nonvolatile writeable memory having an erased-cell reference level and a programmed-cell reference level, the nonvolatile writeable memory having a plurality of memory cells, each of the memory cells being in an erased state when storing a charge below the erased-cell reference level, and each of the memory cells being in a programmed state when storing a charge above the programmed-cell reference level, the method comprising the steps of:

(a) identifying a memory cell having a charge above the erased-cell reference level and below the programmed-cell reference level; and

(b) programming the memory cell until the charge of the memory cell is above the programmed-cell reference level.

(Claim 38 has been cancelled)

39. A method of improving data retention within a non-volatile writeable memory, the method comprising the steps of:

(a) identifying a group of one or more memory cells having a stored charge over a first threshold and less than a second threshold; and

(b) programming each memory cell of the group of one or more cells until each of the memory cells has a stored charge over the second threshold.

40. The method of claim 39 wherein the first threshold corresponds to an erased-cell reference level plus a guardband level.

41. The method of claim 37 wherein the identifying corresponds to identifying a memory cell having a charge above the erased-cell reference level plus a guardband level.

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42. A method of improving data retention in a nonvolatile writable memory having a first reference level and a second reference level, the nonvolatile writable memory having a plurality of memory cells, each of the memory cells being in an first state when storing a charge below the first reference level, and each of the memory cells being in a second state when storing a charge above the second reference level, the method comprising:

writing into each of a set of the plurality of memory cells a respective data value, wherein the data values are one of the first and second states;

identifying a memory cell of the set having a charge above the first reference level and below the second reference level; and

rewriting the respective data value into the memory cell.

43. The memory of claim 42, further having a third reference level intermediate between the first and second reference levels, wherein the identifying comprises identifying a memory cell of the set having a charge above the third reference level and below the second reference level.

44. The memory of claim 43, further having a fourth reference level intermediate between the second and third reference levels, wherein the identifying comprises identifying a memory cell of the set having a charge above the third reference level and below the fourth reference level.

45. The memory of claim 42, wherein the rewriting comprises determining the respective data value to rewrite into the data cell using error correction code.

46. A method of improving data retention in a nonvolatile writable memory having a first reference level and a second reference level, the nonvolatile writable memory having a plurality of memory cells organized into sectors, each of the memory cells being in an first state when storing a charge below the first reference level, and each of the memory cells being in a second state when storing a charge above the second reference level, the method comprising:

accessing a first sector of said memory cells;

identifying a second sector of said memory cells having one or more memory cells with a charge above the first reference level and below the second reference level; and

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rewriting the data values stored in the memory cells of the second sector.

47. The memory of claim 46, wherein said accessing a first sector of said memory cells comprises programming data values into said memory cells of the first sector, wherein the data values are one of the first and second states

48. The memory of claim 46, wherein said accessing a first sector of said memory cells comprises reading the data values stored in said memory cells of the first sector, wherein the data values are one of the first and second states

49. The memory of claim 46, wherein said second sector is chosen at random prior to said identifying.

50. The memory of claim 46, wherein a memory cells of said first sector shares a common bit line with a memory cell of said second sector.

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